MEMORANDUM OF UNDERSTANDING

This Memorandum of Understanding (MOU) is made on 31/07/ 2015 between:

a) The President of India acting through the **Department of Electronics and Information Technology**, Ministry of Communications and Information Technology, Electronics Niketan, 6, CGO Complex, New Delhi-110003 (hereinafter referred to as **DeitY**, which expression shall, unless excluded by or repugnant to the context, be deemed to include his successors in office and assigns) of the FIRST PART;

AND

b) **National Institute of Technology, Hamirpur** (hereinafter referred to as **the institute**) which expression shall, unless excluded by or repugnant to the context, be deemed to include his successors in office and assigns of the SECOND PART. National Institute of Technology, Hamirpur would be a Participating Institution (Category II) under the Programme.

AND

c) **Central Electronics Engineering Research Institute (CEERI), Pilani** a constituent laboratory of Council of Scientific and Industrial Research (CSIR) under Department of Scientific and Industrial Research, Ministry of Science & Technology, Govt. of India (hereinafter referred to as Program Coordination Institute (PCI), which expression shall, unless excluded by or repugnant to the context, be deemed to include his successors in office and assigns) of the THIRD PART.

WHEREAS DeitY has sponsored a Program entitled "Special Manpower Development Programme for Chips to System Design" (hereinafter referred to as the SMDP-C2SD) under the 'Digital India Programme', to be implemented by Ten Resource Centres (RCs) and Fifty Participating Institutes (PIs) (List of RCs and their association with PIs at Annexure-II) over a period of 5 years.

AND WHEREAS, the objectives of the Programme are as follows:

i. Bring in a culture of System on Chip / System designing by developing working prototypes with societal applications using mostly in-house designed ASICs / ICs
ii. Capacity building in the area of VLSI/ microelectronics and Chip to System development.
iii. Broaden the base of ASIC / IC designing in the country
iv. Broaden the R&D base of Microelectronics / Chip to System through 'Networked PhD' program
v. Promote 'Knowledge Exchange Program'
vi. Protection of "Intellectual Property' generated in the program

The various components of the project are outlined in the Administrative Approval of the Programme (Annexure V).

NOW THEREFORE in consideration of the premises and mutual covenants hereinafter contained, the parties hereto agree as follows:

GC (R&DE) Office
Diary No. 387
Date 11/5/15

63/Hon'ble mon
11/5/15

1. DEFINITIONS

Unless otherwise stated, for the purpose of this MOU:

(i) **Articles**: Any Clause of this MOU or partial clause with separate marginal number as referred to anywhere in the workings of this MoU or its Annexures.
(ii) **Category**: Categories of institutions as defined in Annexure I
(iii) **Chip Center**: Centre who will coordinate fabrication of the Integrated Circuits and related activities
(iv) **CI**: Chief Investigator
(v) **Co-CI:** Co-Chief Investigator
(vi) **DeitY**: Department of Electronics and Information Technology, Government of India having its office at 6, CGO Complex, New Delhi - 110003.
(vii) **GIA**: Grants-in-Aid.
(viii) **IEP:** Instruction Enhancement Programme for faculty of Participating Institutions
(ix) **Implementing Agencies**: Ten Resource Centers (RCs) and Fifty Participating Institutes (PIs) (List of RCs and their association with PIs at Annexure-II)
(x) **India Chip Program**: Fabrication of ASICs / ICs under the Program
(xi) **Institute**: is the institute which is 'Second Part' of the MOU
(xii) **IPR**: Shall mean all rights, benefits, title or interest in or to any Intellectual Property (whether registered or not and including all applications for the same).
(xiii) **Annexure**: Any annexure to this MOU as enumerated and cross-referred in these articles.
(xiv) **NSC**: National Steering Committee
(xv) **PCI** : Program Coordination Institute
(xvi) **PI**: Participating Institution (List of PIs at Annexure-II)
(xvii) **Party/Parties** means DeitY or/and Program Coordination Institute or/and the institute
(xviii) **Program**: Will mean the program entitled **"Special Manpower Development Programme for Chips to System Design"**.
(xix) **RC**: Resource Centre (List of RCs at Annexure-II)

2. SCOPE OF MEMORANDUM OF UNDERSTANDING

The Articles 1 to 15 and **Annexure I to VI** to this MOU form an integral part of the MOU between the parties. The terms herein referred in the MOU and Annexures shall be binding on the parties. The MOU together with the Annexures indicates the responsibilities and obligations of the parties to this MOU including terms and conditions, financial arrangement, intellectual property rights, monitoring mechanism etc. of the Program.

3. BROAD IMPLEMENTATION FRAMEWORK

The Department has approved "Special Manpower Development Programme for Chips to System Design" under which CEERI, Pilani has been assigned the role of a Program Coordination Institute (PCI) and a Resource Centre. Under the current Program, the PCI created under CEERI, Pilani (hereinafter referred to as PCI) would be suitably augmented to operate and coordinate the Program in all the RCs and PIs covered under the Program including transfer of funds to the implementing agencies under the Program in a transparent manner. A separate savings bank account will be created by the PCI for the Program. The following are the salient features of implementation framework of the Program:

3.1 The Program would be implemented at 60 institutions i.e. 10 Resource Centres (RCs) and 50 Participating Institutes (PIs). The implementing agencies have been categorized based

on the activities to be undertaken. The category wise table indicating the names of Resource Centres and Participating Institutions is at **Annexure–I**. The implementation structure will be similar to Special Manpower Development Programme- Phase II (SMDP-Phase II) project implemented earlier by DeitY, where Participating Institutions (PIs) were associated with Resource Centers (RCs). The RC-PI cluster proposed under the programme is at **Annexure-II**. The Resource Centers will be the mentoring institutions for the Participating Institutions attached with them under the program. Though a PI will be attached to one of the RCs but depending on the requirement/expertise, support may also be provided by other RCs. Some of the Participating Institutions (Category II) which were there in Special Manpower Development Programme Phase-II may also mentor new Participating Institution (Category III of Annexure –I) based on later's request. The deliverables of the Program are at **Annexure –III**.

3.2 The Resource Centres will review and monitor the progress of Clusters of PIs associated with them. The Resource Centers in particular will help the PIs in - establishing the complete EDA Tool Chain (particularly for the new PIs), identifying the ASIC designs / FPGA Board Level Designs etc. Under the Networked PhD Program, pool of faculty would be constituted in identified verticals from Resource Centres. This pool of faculty will be the 'Mentoring Guide' for the Researchers at PI for Networked PhD activity. Also, Resource Centres would take the lead role either individually or jointly with PIs in submitting proposals that are product oriented in identified areas with societal applications including those identified by Core Advisory Group for Research and Development (R&D) in Electronics Hardware (CAREL) and would be demonstrated as a working prototype at the end of the project. The Participating Institutions will implement various activities of the program as per the proposal submitted by them in their respective institutions. The status of the activities of a cluster will be presented by RC to the National Steering Committee.

3.3 **Implementation & Monitoring of the Programme:**

(i) Monitoring, reviewing and steering of the program will be through two-tier mechanism. At the apex level a National Steering Committee (NSC) will be constituted with Secretary DeitY as its Chairman. The NSC will be responsible for overall implementation and steering of the program. NSC will carryout a mid-term review at the end of third year of the program, recommend suitable amendment/revision in the scope of the program and also suggest suitable implementation strategies. Each implementing agency would be required to submit a project proposals in prescribed proforma, on development of a working prototype of a system / SoC / ASIC/ ICs/ FPGA based designs as well as number and type of manpower they will generate, to the PCI. The proposal received by the PCI will be circulated to the domain Expert Committee constituted by the PCI in consultation with DeitY. The proposal, after incorporating suggestions if any by the Expert Committee, would be submitted to the National Steering Committee for approval.

(ii) NSC will approve the hardware / software / EDA tools proposed to be procured for the implementing agencies based on the proposals submitted by them to develop the system / sub-system / System-on-Chips (SoCs) / ASICs/ ICs / FPGA Based Board Level Designs under the program, likely class size of M. Tech / B. Tech and Number of PhDs. The NSC will regularly review the progress and achievements of the RCs and PIs and recommend release of funds to the PCI, depending on the activities to be undertaken. PCI will release funds to the respective institutions (RCs and PIs) based on the recommendation of the NSC/PRSG. The NSC would approve redistribution of funds, identifying new institutions that could be inducted in the programme based on the availability of resources etc. Also, NSC may, during the course of implementation of the project, evolve and recommend initiation of new activities in line with the aims of the program. NSC will also recommend proposals under Knowledge Exchange Program and may designate specific responsibilities to RCs, PIs and the PCI to ensure smooth implementation and progress of the programme.

(iii) **Project Review and Steering Groups** (PRSGs) would review and steer the progress of activities of the RCs and PIs, ensure time-bound implementation of the project and recommend to NSC release of funds from second and subsequent installments in respect of each implementing agency.

Five PRSGs would be constituted for the 10 Clusters. Thus, one PRSG will monitor the progress of two RC / PIs clusters. Chairmen of these PRSGs would be the members of the National Steering Committee who will apprise NSC about the progress of institutions.

(iv) Subsequent to signing of an MoU with DeitY for implementation of the Program, the institute would submit a project proposal in a prescribed format and nominate a faculty member as Chief Investigator (CI) and a Co-Chief Investigator (Co-CI) to act as a single point of contact with PCI/DeitY. The Chief Investigator and Co-Chief Investigator, who will be responsible for implementation of the project, should be from Electronics/Communication/ Computer Science & Engineering department where Electronics stream is being taught.

(v) The project proposal submitted by the implementing agencies and as approved by NSC, would be provided with the first installment of Grant-in-aid through PCI. Thereafter, depending on the target met, the subsequent installments would be released to the implementing agencies on an annual basis subject to receipt of Utilization Certificate of previous grants and based on the recommendations / approval of PRSG / NSC.

(vi) Further, an impact assessment of the Program would be carried out by a third party, like Indian Institute of Management, in the 3rd year of the Program so that mid-course corrections, if any, could be carried out during the balance period of implementation of the Program.

4. RESPONSIBILITIES OF DEITY, PROJECT COORDINATION INSTITUTE (PCI) AND IMPLEMENTING AGENCIES (both Resource Centres and Participating Institutions)

4.1 Responsibilities of DeitY

i. Constitute National Steering Committee
ii. Set up 5 Project Review and Steering Group (PRSG)
iii. Release grant-in-aid to PCI on the recommendations of PRSG and NSC as per the plans approved by DeitY
iv. Assist in expediting issues related to the progress of the Program including co-ordination with the relevant Govt. departments/ organizations/ institutions/ PCI and other agencies concerned.
v. Screening of proposals sought by PCI for setting up of Chip Centre before they are submitted to NSC
vi. Screening of proposals sought by PCI for development of System/ Sub-systems/ SoCs/ ASICs/ ICs/ FPGA before they are submitted to NSC.
vii. To take up any other issues and aspects related to the Program.

4.2 Responsibilities of PCI:

Following would be the responsibilities of PCI:

i. Obtain Memorandum of Understanding from all the RCs and PIs and facilitate signing of MoUs between DeitY with RCs and PIs.
ii. Release GIA to all the institutions participating in the Programme based on the approval of NSC/PRSG and as per directions of DeitY
iii. PCI will regularly liaison and coordinate with all RCs, PIs, Chip Centre and support DeitY in implementation and monitoring of the Program at the RCs and

PIs and be the single point of contact on behalf of DeitY w.r.t. implementation of the Program

iv. Seek project proposals from all the RCs and PIs for design of systems / sub-systems/SoCs/ ASICs/ FPGA based Board Level Designs and put up to NSC for consideration and approvals

v. Seek project proposals from all the Implementing Agencies for setting up of Chip Centre

vi. Obtain requirement of funds and Utilization Certificates and Audited Statement of Accounts from all the RCs and PIs and submit a composite UC and audited statement of accounts to DeitY.

vii. Coordinating Faculty Exchange Program / Paper Presentation in International Conferences by students and researchers of RCs and PIs

viii. Facilitate patenting of research work carried out under the Program

ix. Constitute committees of experts consisting of faculty from RCs i.e. the 'Mentoring Guides' and industry for Defining PhD research problems for researchers in PIs in consultation with their respective guides, organize separate session for interaction of researchers with the experts to address their issues during the yearly conferences / seminars / symposium and coordinate Networked PhD Program

x. Coordinate activities like conducting /scheduling – short term courses / IEPs / yearly workshops / seminars / ZoPP workshops etc. and seek proposals from the Resources Centres for organizing IEPs

xi. Coordinate Development of Model Syllabus oriented towards System-on-Chip/ System design

xii. Bring out periodic progress report, maintain technical and financial database of the project activities and collect any other relevant data for monitoring of the Program. Technical and financial status of Implementing Agencies supported under the project will be maintained by PCI and provided to DeitY.

xiii. To facilitate carrying out an impact assessment of the Program by a third party in the third year of the Program

xiv. Coordinate the meetings of the NSC as well as Project Review and Steering Groups.

xv. Coordinate any other related activity assigned by DeitY / NSC for the smooth implementation of the project. The PCI shall ensure that all the activities of the Program are completed strictly as per timelines.

4.3 Responsibilities of Implementing Agencies (RCs and PIs):

4.3.1 GENERAL

i. The implementing agencies will nominate Chief Investigator and Co-Chief Investigator who will coordinate all the activities under the programme. CI and Co-CI would liaise with PCI, DeitY, industry, Chip centre and other implementing agencies and ensure that deliverables of the project are achieved in a time bound manner.

ii. Implement the various activities of the program in its institution as per the proposal submitted by it under the Programme.

iii. Accept the directions provided by the NSC/PRSG/DeitY/PCI for implementation of the project.

iv. Submit periodic information on technical and financial progress of the project, utilization certificate and audited statement of account to PCI/ PRSG and DeitY in time as per format for monitoring the implementation of the Program.

v. The implementing agencies will provide the required inputs to DeitY and PCI in time and PIs would ensure all support to its respective mentoring RC for smooth functioning of the Programme.

vi. The implementing agencies would make available the NKN facility in their institution for the Programme.

vii. The implementing agencies will provide adequate built-up space for housing the equipment and also necessary faculty and facilities for smooth implementation of the project. The implementing agencies would involve Electronics/ Communication Department/ Computer Science & Engineering Department for smooth implementation of the project. However the laboratory(ies) under the project would be set up only in one Department where Electronics stream is being taught. However, in case of any genuine difficulty(ies), the change would be decided after obtaining consent of DeitY in writing as per para 14 of this MoU.

viii. The implementing agencies will ensure that the contract faculty and the staff assigned for the project will work full time for the project. Positions created under this project will be purely on temporary basis for the duration of the project and DeitY would have no liability whatsoever for sustaining such temporary staff after completion/termination of the project.

ix. The contract faculty and the staff assigned for the project will not be transferred to any other project/institution.

x. The implementing agencies will ensure that the equipment and other infrastructure is in proper working order.

xi. The implementing agencies would maintain financial and other records as per norms and procedures laid down by DeitY for the project. They would send information relating to the project to PCI/DeitY (in case of PIs – also to the RC associated with them) when called for.

xii. No commercial use will be made of the infrastructure created, equipment/training material etc procured/supplied/developed under the project without the prior approval of DeitY. Any liability for violation would have to be borne by the implementing agencies and may also result in termination of the project.

xiii. All the items received under the project will be entered in the appropriate Stock Registers. "Special Manpower Development Programme for Chips to System Design, Department of Electronics & Information Technology (Govt. of India)" would be suitably displayed on the items. Responsibility for safe keeping of all the assets will be that of the implementing agencies. Loss and theft of any equipment/items supplied under this project would be reported to appropriate authority. Proper investigation by concerned authority would be carried out and appropriate action would be taken. The same will be reported to DeitY / PCI.

xiv. All the assets (i.e. equipment, lab infrastructure, course material, books etc.) created/procured as part of the project funds would be the property of DeitY. At the end/termination of the project, the Department of Electronics & Information Technology would decide on the future use of such assets.

xv. The terms and conditions of the grant-in-aid as per Annexure-VI would form part of the MOU.

xvi. The implementing agencies would sign any agreement(s) as may be required with the supplier(s) of hardware and software and implementing agencies would be solely responsible for any liability(ies) arising due to breach of such agreement(s).

xvii. The implementing agencies would also agree to utilize the VLSI laboratory(ies) set up under this project for carrying out any sponsored R&D projects sponsored by DeitY in the area of VLSI design & related software.

xviii. The Head of the institution of the implementing agencies will make all efforts to ensure that the procedures of the institution do not come in the way of smooth implementation of the project and, if necessary, provide special dispensation for this purpose.

xix. In case faculty/student/researchers use the VLSI Lab setup under this project for carrying out technical activities, including publishing papers, which are not supported by DeitY, they will acknowledge DeitY's name and will inform the Department accordingly.

4.3.2 TECHNICAL MATTERS

4.3.2.1 Responsibilities of RCs (Category I)

(i) Submission of proposal

a) RC would submit project proposals in the prescribed format for development of working prototype of SoC/System/Sub-System and generation of specialized manpower for evaluation and approval by NSC.
b) Resource Centers may submit the proposal either individually or in a consortium mode jointly with PIs from within their identified cluster for the development of working prototypes of systems / sub-systems / SoCs
c) The allocation of hardware, software, EDA tools to RC will be based on the proposal submitted by it to NSC.
d) Resource Centres will involve industry experts for identification of system/product oriented projects.

(ii) Courseware development on 'System / SoC / Product Development'

RC will participate in preparing model syllabus oriented towards System/SoC/Product Development involving other experts including experts from industry.

(iii) Instruction Enhancement Programme (IEP) for faculty and Training of Staff

a. Resource Centers would submit proposal to the PCI for organizing IEPs.

b. Identified RC would conduct Instruction Enhancement Program (IEP) for the faculty and training program for staff of the project/research scholars of PIs as per schedules drawn up by PCI/DeitY.

(iv) Network PhD Activity and Exchange Program

a) Enrol researches under Network research Program

b) Pool of faculty from Resource Centres in identified verticals to be called 'Mentoring Guides' will be constituted. The researchers enrolled under the Network PhD program at the participating institutions and their guides would be mentored by these 'mentoring Guides'.

c) The RCs will submit proposal online either individually or jointly for bilateral collaboration with foreign institute that have experience and expertise in system development. The bilateral collaboration could have linkages with faculty / researcher exchange program.

d) Researchers / faculty may submit proposals for research exchange program

e) Students / Researchers / faculty may submit proposals for presenting papers in International Conferences of repute like IEEE

(v) Making available necessary infrastructure

RCs would provide/establish the necessary infrastructure for housing the equipment, furniture, books, journals etc to be provided for various laboratory & related facilities and library under the project.

(vi) Industrial attachments

RCs would ensure regular interaction with the industries by making students work on projects proposed by the industries, having part-time and/or short-term experts from the industry participating at the institution in different roles like assist in working out research problem for 'Networked PhD'. RCs will also involve industry experts for identification of projects for development of working prototypes of systems / sub-systems / SoCs having societal relevance. They would agree to abide by the DeitY guidelines in this regard.

(vii) India Chip Programme

a) Resource Centres will send the student designs in required format and media for prototyping under India-Chip Programme as per schedule announced by Chip Centre. The design details would be submitted online in the prescribed format to the Chip Centre. The Chip Centre will be responsible for the fabrication of the Integrated Circuits.

b) After receipt of the packaged chips, design team at the concerned Resource Centre should submit its chip testing report to the Chip Centre.

c) The details of proven designs like functionality, usage modes, limitations, characterization data etc. of the IP cores generated by Resource Centres will be submitted 'online' to the Repository setup at the Chip Center.

d) For carrying out characterization and testing of the fabricated chip, facilities at the Chip Centre would be utilized. In case, some facilities are not available at chip center, services of external agencies could be taken with concurrence of the Chip Centre.

(viii) Web based hosting of educational material

Resource Centre would host the material developed by them on the program website or make the contents available to the centralized web administrator for hosting them on the website. RC would be provided web based administration for the same.

(ix) Patents / Copyright / Registration

Patents / Copyright / Registration should be obtained for all the IPs generated under the program. The reference designs and information about the IP cores developed will be made available to the repository for their possible use/re-use by the designers.

(x) ZOPP Workshop

RC would conduct at least one ZOPP workshop as per the schedule drawn up by the PCI/DeitY. The Chief Investigator should make detailed presentation of the activities undertaken under the programme and their status.

(xi) Any other responsibility under the scope of the project assigned by NSC for fulfilling the aims & objectives of the program

4.3.2.2 Technical Supports by Resource Centres with respect to Participating Institutions within the RC-PI cluster (as per Annexure II) and Monitoring of the progress of the work at PIs.

(i) RC will help in detailed planning of the laboratories, and other facilities to be setup under the program for PIs, particularly new PIs attached to them and establishing the laboratory and related facilities after the requisite equipment arrived in respective PIs.

(ii) Work very closely with the faculty of the Electronics/Electronics & Communication/Computer Department of the PIs attached to the RC for implementation of various components of the project.

(iii) Assist the PIs in identifying projects at the graduate and undergraduate level, and in setting up procedures and practices for effective implementation of the project.

(iv) Work closely with the faculty of the PIs in establishing close informal/formal linkages with industries in the vicinity.

(v) Assist PIs in initiating M.E./ M. Tech program in VLSI / Embedded System at Participating Institutions within three years of initiation of the project if not already initiated in the Institution wherever it is not offered.

(vi) Resource Centre would monitor progress of implementation of each activity of the project at the Participating Institutions attached to them and would submit a quarterly report to the PCI/DeitY. Resource Centre will be the mentoring institutions for the Participating Institutions associated with them under the program

(vii) Resource Centre will visit the PIs attached to them at least once every year.

(viii) Resource Centre would help PIs in identifying the ASIC designs / FPGA Board Level Designs, which could be designed by Pis especially those designs which could be part of Systems / sub-systems/SoCs (System-on-Chips) proposed to be jointly developed under the program

(ix) Resource Centres would present the status of the PIs of the cluster, attached to them, to the NSC

4.3.2.3 Expected Deliverables from RCs (Category I)

(i) **Expected Manpower Generation:**

Following manpower would be generated under the program by each RC (the manpower indicated here is tentative based on the experience of Special Manpower Development

Program – Phase II, however, the institute may indicate the likely manpower which will be generated under different categories at Annexure IV):

Year	1st	2nd	3rd	4th	5th	Total
Type IV	141	141	141	141	141	705
Type III	35	35	35	35	35	175
Type II	19	19	19	19	19	95

Type-I Atleast 3 researchers (mix of part-time and full time PhD) per year would be enrolled in the identified verticals over and above the researchers enrolled under MHRD.

(It may be noted that the resources allocated to the institute would depend on the manpower generated under the program by the institute)

The funds for researchers enrolled under the Networked PhD Program researchers, would be provided under the Department's Scheme entitled "Scheme to give a thrust to research in areas of Electronics System Design and manufacturing and IT/IT Enabled Services (ITES)".

(ii) **Development of working prototypes of Systems / Sub-system / SoCs**

Each RC will develop at least one (1) working prototype of a system/sub-system/SoC using mostly the ASICs/ICs designed in-house.

(iii) **IPR**

At least one (1) IP core will be generated under the program and details submitted online to the Repository to be setup at the Chip Center.

(iv) **Publications**

At least thirty (30) papers should be published in journals and conference for the work carried out under the program.

(v) **Collaborative Developments**

One research and development project with foreign universities to be undertaken keeping system development in mind.

(vi) **Model Syllabus**

Curriculum/syllabus oriented towards 'System / SoC and Product Development' should be developed in consultation with all the other RCs. Efforts should be made to offer this course in the RC with the approval of competent authority.

4.3.2.4 Responsibilities of PIs (Category II)

(i) Submission of proposal

a) PI would submit project proposals in the prescribed format for development of ASIC in consultation with their mentoring RCs to PCI for evaluation by NSC. PI may submit this

proposal in consortium mode with its mentoring RC where the ASIC may be part of the working prototype being developed by the RC. The proposal should indicate expert manpower likely to be generated under the program.

b) The proposals would clearly indicate the activities these institutions would carryout under the program.
c) The allocation of hardware, software, EDA tools to the PI will be based on the proposal approved by NSC.
d) PI will involve industry experts for identification of system/product oriented projects particularly those having societal relevance.

(ii) Courseware on 'System / SoC / Product Development'

PI will make every effort to bring the Model Syllabus oriented towards 'System / SoC / Product Development' developed by RCs into use in their regular teaching.

(iii) Instruction Enhancement Programme for faculty and Training of Staff Programmes

PIs would send their faculty and staff assigned to this project for attending courses under the Instruction Enhancement Programme for faculty and training of Staff Programme as per schedule drawn up by PCI/DeitY.

(iv) Network PhD Activity and Exchange Program

a) The PI would enrol researchers under Networked PhD Program. The researchers enrolled under the Network PhD program at the participating institutions and their guides would be mentored by the 'Mentoring Guides' in identified verticals from Resource Centers.
b) The PIs may submit proposal online either individually or jointly with RCs for bilateral collaboration with foreign institute that have experience and expertise in system development. The bilateral collaboration should have linkages with faculty / researcher exchange program.
c) Researchers / faculty may submit proposals for research exchange program
d) Students / Researchers / faculty may submit proposals for presenting papers in International Conferences of repute like IEEE

(v) Making available necessary infrastructure

PIs would provide/establish the necessary infrastructure for housing the equipment, furniture, books, journals etc to be provided for various laboratory & related facilities and library under the project.

(vi) Industrial attachments

PIs would ensure regular interaction with the industries by making students work on projects proposed by the industries, having part-time and/or short-term experts from the industry participating at the institution in different roles like assist in working out research problem for 'Networked PhD'. They would agree to abide by the DeitY guidelines in this regard.

(vii) Continuing Engineering Education Programme

Based on DeitY's inputs, PIs would conduct Continuing Engineering Education Programme (CEEP) for the in-service personnel (i.e. practicing Engineers and Technicians)

(viii) India Chip Programme

a) PI will send the student designs in required format and media for prototyping under India-Chip Programme as per schedule announced by Chip Centre. The design details would be submitted online in the prescribed format to the Chip Centre. The Chip Centre will be responsible for the fabrication of the Integrated Circuits.

b) After receipt of the packaged chips, design team at the concerned Resource Centre should submit its chip testing report to the Chip Centre.

c) The details of proven designs like functionality, usage modes, limitations, characterization data etc. of the IP cores generated by Participating Institute will be submitted 'online' to the Repository setup at the Chip Center.

d) For carrying out characterization and testing of the fabricated chip, facilities at the Chip Centre would be utilized. In case, some facilities are not available at chip center, services of external agencies could be taken with concurrence of the Chip Centre.

(ix) Initiation of M. Tech Program in VLSI/Embedded Systems/Product Design

Participating Institution would offer M.E/M. Tech programme in VLSI design / Embedded Systems with the approval of their competent authorities within the first three years of initiation of the project where such program is not being offered by the Institution.

(x) Web based hosting of educational material

Participating Institution would host the material developed by them on the programme website or make the contents available to the centralized web administrator for hosting them on the programme website. PI would be provided web based administration for the same.

(xi) Patents / Copyright / Registration

Patents / Copyright / Registration should be obtained for all the IPs generated under the program. The reference designs and information about the IP cores developed will be made available to the repository for their possible use/re-use by the designers.

(xii) ZOPP Workshop

The Participating Institution should send the Chief Investigator and the Co-Chief Investigator to attend the ZOPP Workshop as per the schedule drawn by PCI. The Chief Investigator should make a detailed presentation of the activities undertaken under the project and their status.

(xiii) Participating Institutions may also mentor new Participating Institution (Category III) based on later's request

(xiv) Any other responsibility under the scope of the project assigned by NSC for fulfilling the aims & objectives of the program

4.3.2.5 Expected Deliverables from PIs (Category II)

(i) Manpower Generation

Following manpower would be generated under the program by Participating Institute (the manpower indicated here is tentative based on the experience of Special Manpower Development Program – Phase II, however, the institute may indicate the likely manpower which will be generated under different categories at Annexure IV):

Year	1st	2nd	3rd	4th	5th	Total
Type IV	141	141	141	141	141	705
Type III	35	35	35	35	35	175
Type II	19	19	19	19	19	95

Type-I Atleast 1 researches (full time / part time PhD) per year would be enrolled under the Networked PhD Program in the identified verticals over and above the researched enrolled under MHRD.

(It may be noted that the resources allocated to the institute would depend on the manpower generated under the program by the institute)

The funds for researchers enrolled under the Networked PhD Program researchers, would be provided under the Department's Scheme entitled "Scheme to give a thrust to research in areas of Electronics System Design and Manufacturing and IT/IT Enabled Services (ITES)".

(ii) Development of working prototypes of system/sub-system/SoC/ASICs:

Participating Institution will develop / design at least two ASICs. The PIs may work with Resource Centers for developing these ASICs which could be used in the Working Prototype of the System / SoC being developed by Resource Center.

(iii) IPR

At least one (1) IP core should be generated under the program and its details submitted online to the Repository of proven designs set up at the Chip Centre.

(iv) Publications

Atleast 10 papers should be published in journals and conference for the work carried out under the program.

4.3.2.6 Responsibilities of PIs (Category III)

(i) Submission of proposal

a) PI would submit project proposals in the prescribed format for development of ASIC/ FPGA based board level design/ or SPICE simulated analog designs in consultation with their mentoring RCs to PCI for evaluation by NSC. PI may submit this proposal in consortium mode with its mentoring RC where the ASIC may be part of the working prototype being

developed by the RC. The proposal should indicate expert manpower likely to be generated under the program.

b) The proposals would clearly indicate the activities these institutions would carryout under the program.
c) The allocation of hardware, software, EDA tools to the PI will be based on the proposal approved by NSC.
d) PI will involve industry experts for identification of system/product oriented projects particularly those having societal relevance.

(ii) Courseware on System / SoC/ Product Development

PI will make effort to bring the Model Syllabus oriented towards 'System / SoC/ Product Development' developed by RCs into use in their regular teaching.

(iii) Instruction Enhancement Programme for faculty and Training of Staff Programmes

PIs would send their faculty and staff assigned to this project for attending courses under the Instruction Enhancement Programme for faculty and training of Staff Programme as per schedule drawn up by PCI/DeitY.

(iv) Network PhD Activity and Exchange Program

a) The PI may enrol researchers under Networked PhD Program. The researchers enrolled under the Network PhD program at the participating institutions and their guides would be mentored by the 'Mentoring Guides' in identified verticals from Resource Centers.
b) The PIs may submit proposal online either individually or jointly with RCs for bilateral collaboration with foreign institute that have experience and expertise in system development. The bilateral collaboration should have linkages with faculty / researcher exchange program.
c) Researchers / faculty may submit proposals for research exchange program
d) Students / Researchers / faculty may submit proposals for presenting papers in International Conferences of repute like IEEE

(v) Making available necessary infrastructure

PIs would provide/establish the necessary infrastructure for housing the equipment, furniture, books, journals etc to be provided for various laboratory & related facilities and library under the project.

(vi) Industrial attachments

PIs may facilitate regular interaction with the industries by making students work on projects proposed by the industries, having part-time and/or short-term experts from the industry participating at the institution in different roles like assist in working out research problem for 'Networked PhD'.

(vii) Continuing Engineering Education Programme

Based on DeitY's inputs, PIs would conduct Continuing Engineering Education Programme (CEEP) for the in-service personnel (i.e. practicing Engineers and Technicians) as per directions of PCI.

(viii) India Chip Programme (only if an ASIC design is undertaken by PI)

a) Participating Institution may send the ASIC designs in required format and media for prototyping under India-Chip Programme as per schedule announced by Chip Centre. The design details would be submitted online in the prescribed format to the Chip Centre. The Chip Centre will be responsible for the fabrication of the Integrated Circuits.
b) After receipt of the packaged chips, design team at the concerned Resource Centre should submit its chip testing report to the Chip Centre.
c) The details of proven designs like functionality, usage modes, limitations, characterization data etc. of the IP cores generated by Participating Institute will be submitted 'online' to the Repository setup at the Chip Center.
d) For carrying out characterization and testing of the fabricated chip, facilities at the Chip Centre would be utilized. In case, some facilities are not available at chip center, services of external agencies could be taken with concurrence of the Chip Centre.

(ix) Initiation of M. Tech Program in VLSI/Embedded Systems/Product Design

Participating Institution would offer M.E/M. Tech programme in VLSI design / Embedded Systems with the approval of their competent authorities within the first three years of initiation of the project where such program is not being offered by the Institution.

(x) Web based hosting of educational material

Participating Institution would host the material developed by them on the programme website or make the contents available to the centralized web administrator for hosting them on the programme website. PI would be provided web based administration for the same.

(xi) Patents / Copyright / Registration

Patents / Copyright / Registration should be obtained for all the IPs generated under the program. The reference designs and information about the IP cores developed will be made available to the repository for their possible use/re-use by the designers.

(xii) ZOPP Workshop

The Participating Institution should send the Chief Investigator and the Co-Chief Investigator to attend the ZOPP Workshop as per the schedule drawn by PCI/DeitY. The Chief Investigator should make a detailed presentation of the activities undertaken under the project and their status.

(xiii) Any other responsibility under the scope of the project assigned by NSC for fulfilling the aims & objectives of the program

4.3.2.7 Expected Deliverables from PIs (Category III)

(i) Expected Manpower Generation:

Following manpower would be generated under the program by Participating Institute (the manpower indicated here is tentative based on the experience of Special Manpower

Development Program – Phase II, however, the institute may indicate the likely manpower which will be generated under different categories at Annexure IV):

Year	1st	2nd	3rd	4th	5th	Total
Type IV	110	110	110	110	110	550
Type III	25	25	25	25	25	125
Type II	15	15	15	15	15	75
Type I	Institute may enroll, full time / part time researchers under Networked PhD Program in the identified verticals over and above the researchers enrolled under MHRD.					

(It may be noted that the resources allocated to the institute would depend on the manpower generated under the program by the institute)

The funds for researchers enrolled under the Networked PhD Program researchers, would be provided under the Department's Scheme entitled "Scheme to give a thrust to research in areas of Electronics System Design and manufacturing and IT/IT Enabled Services (ITES)".

(ii) Development of FPGA based digital circuits or SPICE simulated analog designs:

Participating Institution will undertake 2 FPGA based digital circuits or SPICE simulated analog designs in consultation with their mentoring RC.

However, PI may undertake designs of ASIC/ICs in place of FPGA based digital circuits / spice simulated analog designs, in consultation with their mentoring RC.

(iii) IPR

Details of IP Core generated under the program should be submitted online to the Repository of proven designs set up at the Chip Centre.

(iv) Publications

Atleast 2 papers should be published in journals and conference for the work carried out under the program.

5. FINANCIAL DETAILS:

5.1 The Budget outlay of the Program will be Rs. 99.72 Crore spread over a period of 5 years to be implemented by implementing agencies as Grant-in-aid from DeitY. The relevant details are at **Annexure-V**.

5.2 The financial support to the institute would be as per following:

i. The allocation of hardware, software, EDA tools to the institute will be based on the proposal submitted by it to NSC

ii. Funds for Manpower, consumables, contingencies, travel and training, books etc. would be provided to the institute as per the Detailed Project Report subject to availability of budget in the financial year. Rest of the activities i.e. fabrication of chips, procurement of hardware, software, EDA tools, multimedia/ teleconferencing equipment would be undertaken centrally.

iii. The institute will maintain a separate savings bank account for the project in any public sector bank to which all money provided by DeitY under the project shall be credited. The interest earned on this account will be treated as a credit to grantee to be adjusted towards future installments of the grant/refunded to DeitY.

iv. The accounts will be operated, utilized and audited as per the norms and procedures followed by the institute. The institute will send the audited statement of accounts and the utilization certificates to PCI as prescribed by DeitY annually.

v. The accounts to be maintained by the institute towards this project will be open to be seen/verified/audited by DeitY or any of its designated authority or by the party from C&AG's office.

5.3 The Grants-in-Aid will be regulated in accordance with the provisions contained in Chapter 9 of the General Financial Rules, 2005, as amended from time to time, read with the Government of India's decisions incorporated there-under, and any other guidelines which may be issued in this regard. The institute would also be required to accept and sign the standard Terms & Conditions of Grants-in-Aid of DeitY **(Annexure-VI)**. All financial transactions will be subject to the requirements of the *Fiscal responsibility & Budget Management Act*.

5.4 **Broad guidelines for release of GIA:**

(i) The fund release for the 1st installment would be made to the institute subject to signing the MoU and approval of proposal submitted to NSC.

(ii) All subsequent releases to be based on the recommendations of the Project Review & Steering Group (PRSG) and National Steering Committee (NSC) and as per directions of DeitY. Sole criteria for release of funds would be targets met under the Program and subject to receipt of Utilization Certificate for the previous installment(s).

6. APPOINTMENT OF CHIEF INVESTIGATOR & CO-CHIEF INVESTIGATOR

To ensure the successful implementation of the Program, the institute will appoint a Chief Investigator and a Co-Chief Investigator for the Program. The Chief Investigator will have the overall responsibility of the implementation of the Program. During the period the Chief Investigator is not available, the Co-Chief Investigator will perform the duties of the Chief Investigator. **The Chief and Co-Chief Investigator of the Program will not be changed as far as possible during the course of the Program.**

7. DURATION OF THE PROGRAM

The Program duration is of 5 years from the date of issue of Administrative Approval. Any need for its extension, if essential, will be reviewed by the PRSG and NSC for its further consideration and approval by DeitY. However, it would be the endeavor of all the parties to this MOU to complete the Program within the stipulated period. DeitY will not bear any

expenditure towards recurring, upgradation or maintenance expenses after the completion of the Program.

8. COMPLETION OF PROGRAM

The Project shall be deemed to have been successfully completed when the institute achieves the desired objectives of the Program as brought out in this MOU. The institute will submit a Project Completion Report and a composite audited statement of accounts within one month of the completion of the Program.

9. INTELLECTUAL PROPERTY RIGHTS (IPR)

The institute will ensure that the Intellectual Property generated under the Program is protected. The Intellectual Property and the rights associated with it would be regulated by the Terms and Conditions governing Grant-in-Aid (**Annexure – VI**).

10. CONFIDENTIALITY

The institute undertakes on its behalf to maintain strict confidentiality of the Program including, but without limitation to, the R&D work and know-how generated and prevent, disclosure thereof, for any purpose, other than in accordance with this MOU. DeitY and PCI, in turn, will also ensure confidentiality as required for the Program. The provisions of this clause will outlive this MOU.

11. FORCE MAJEURE

None of the parties shall be held responsible for non-fulfillment of their respective obligations under this MOU due to the exigency of one or more of the force majeure events such as, but not limited to, Acts of God, war, flood, earthquakes, strike, lockouts, epidemics, riots, civil commotion etc., provided on the occurrence and in cessation of any such event, the party affected thereby shall give a notice in writing to the other party immediately after but not later than one month of such occurrence and cessation. The period between the occurrence and cessation of such event will be excluded while calculating the period during which the party has to perform his obligations under this MOU. If the force majeure conditions continue beyond six months, the parties shall then mutually decide about the future course of action.

12. TERMINATION OF THE PROGRAM

(i) DeitY will have the right to terminate the MOU based on recommendation of the PRSG/NSC at any stage, if it is satisfied that:
   (a) the money released has not been properly utilized, or
   (b) appropriate progress on the Program is not being made, or
   (c) the Program is not being carried out as per the terms and conditions and/ or as per the nature and scope of work as defined in the approved Program proposal.

(ii) If the institute faces difficulties in implementing the Program for any techno economic and reasons other than the above, based on the recommendations of the NSC and PRSG and as directed by DeitY, the institute shall pay back all unspent DeitY grants released.

(iii) If the institute abandons the Program on its own without approval of DeitY, then DeitY will have the right to recover the funds disbursed to the institute.

13. VALIDITY

13.1 The duration of this MOU will be for a period of 5 years from the date of Administrative Approval or till completion of the Program, whichever is later.

13.2 Any matter not covered specifically in the MOU may be settled by mutual agreement. On points of disagreement, the matter may be referred to Secretary, DeitY for a decision, which shall be final and binding on all the parties.

14. MODIFICATIONS TO THE MEMORANDUM OF UNDERSTANDING

The MOU can be modified through mutual written consent of all the parties to this MOU.

15. SEAL OF PARTIES

In witness whereof the parties hereto have signed this MEMORANDUM OF UNDESTANDING on the day, month and year mentioned herein before.

Sign: .....
Name (in Block Letters): .....
.....
[For and on behalf of the President of India]
Department of Electronics and Information Technology
Ministry of Communications and Information Technology
Government of India
Electronics Niketan, 6, CGO Complex, New Delhi – 110003.

Sign: 9/2/15
Name (in Block Letters): .....
Prof. Rajnish Shrivastava
[Head of the Institution] Director
National Institute of Technology
Hamirpur, Himachal Pradesh-177 005, India.
Prof. Rajnish Shrivastava
Director
NIT Hamirpur (H.P.)-177005

Sign: .....
Name (in Block Letters): .....
.....
[For and on behalf of Program Coordination Institute]
Central Electronics Engineering Research Institute (CEERI), Pilani – 333031.
डॉ. चंद्रशेखर/Dr. CHANDRA SHEKHAR
निदेशक/Director
सीएसआईआर–केंद्रीय इले.अभि.अनु.संस्थान
CSIR-Central Electronics Engg. Res.Institute
पिलानी(राजस्थान)/Pilani (Raj.) 333 031

IN THE PRESENCE OF WITNESSES

Signature: 9/2/2015
Name: Dr Ashwani Kumar
Occupation: Assoc. Prof., EEE
Address: EE, CEED, NIT, HMR

Signature: 9.2.15
Name: Dr. Vinod Kapoor
Occupation: Dean (Academic)
Address: Prof. (ECE) & Dean (Acad.), NIT HAMIRPUR (H.P.)

Signature: .....
Name: RAJ SINGH
Occupation: CHIEF Sc.
Address: CSIR-CEERI

राज सिंह
Raj Singh
प्रमुख वैज्ञानिक
Chief Scientist
सीएसआईआर–केन्द्रीय इलेक्ट्रॉनिकी अभियांत्रिकी अनुसंधान संस्थान
CSIR- Central Electron-cs Engineering Research Institute
पिलानी (राजस्थान) / Pilani (Rajasthan) 333031

Sunita Verma

SUNITA VERMA
Scientist F
DeitY

सुनीता वर्मा/SUNITA VERMA
वैज्ञानिक 'एफ' /Scientist 'F'
भारत सरकार /Government of India
इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी विभाग
Deptt. of Electronics & Information Technology
इलेक्ट्रॉनिक्स निकेतन, नई दिल्ली-110003
Electronics Niketan, New Delhi-110003

CSIR-CEERI

ANNEXURE-I

CATEGORIES of Institutions Participating in the Program

Category I	Category II	Category III
Resource Centres (10)	**Participating Institutions which were there in SMDP-II and New IITs (which were not earlier in SMDP-II) (30)**	**New Participating Institutions (20)**
1. IIT Kharagpur 2. IIT Bombay 3. IIT Madras 4. IIT Kanpur 5. IIT Delhi 6. IISc Bangalore 7. CEERI Pilani 8. IIT Roorkee 9. IIT Guwahati 10. VNIT Nagpur	**PIs which were there in SMDP-II** 11. NIT Srinagar 12. DBRANIT Jalandhar 13. NIT Hamirpur 14. NIT Kurukshetra 15. Thapar University Patiala 16. MNIT Jaipur 17. MNNIT Allahabad 18. IIT(BHU) Varanasi 19. NIT Durgapur 20. IIEST Howrah 21. Jadavpur University 22. NIT Silchar 23. NIT Jamshedpur 24. NIT Rourkela 25. PSG College of Technology, Coimbatore 26. NIT Warangal 27. NIT Surathkal 28. SVNIT Surat 29. MANIT Bhopal 30. SGSITS Indore 31. NIT Calicut 32. NIT Tiruchirappalli **New IITs** 33. IIT Mandi 34. IIT Ropar 35. IIT Jodhpur 36. IIT Bhubaneswar 37. IIT Gandhinagar 38. IIT Indore 39. IIT Hyderabad 40. IIT Patna	41. NIT Agartala 42. NIT Patna 43. NIT Raipur 44. NIT Sikkim 45. NIT Goa 46. NIT Arunachal Pradesh (Yupia) 47. NIT Meghalaya 48. NIT Nagaland 49. NIT Manipur 50. NIT Mizoram 51. NIT Uttarakhand 52. NIT Delhi 53. NIT Puducherry 54. IIIT Allahabad 55. ABVIIITM Gwalior 56. PDPMIIIT(D&M) Jabalpur 57. IIIT(D&M) Kancheepuram 58. Societies under DeitY (CDAC, NEILIT, SAMEER etc.) 59. University of Calcutta (Dept. of Radiophysics & Electronics) 60. Indira Gandhi Technical University for Women, Delhi

Categorywise activities

S. No.	Category I	Category II	Category III
	Resource Centres (10)	**Participating Institutions which were there in SMDP-II and New IITs (which were not earlier in SMDP-II) (30)**	**New Participating Institutions (20)**
	i) Design, development and demonstration of Working Prototype of Systems /sub-systems / System on Chip (SoCs) ii) Organise Instruction Enhancement Program (IEP) for faculty of PIs and tool Administration IEP for laboratory engineers of RCs and PIs iii) upgrading of VLSI design laboratories iv) Networked PhD Program v) Introduce teaching of various courses on VLSI Design & System level design (BE/B.Tech/ME/M.Tech/ PhD) vi) Prototyping and Siliconization under India Chip Programme/ Chip Center vii) Knowledge exchange programme viii) Web based Dissemination of educational material and setting up of C2S Website and Mirror sites ix) Support for attending national/international conferences x) Organizing Conference/ Workshops / symposium/ ZOPP workshop	i) Design of Application Specific Integrated Circuits (ASICs) ii) Attend Instruction Enhancement Program (IEP) for faculty of PIs and tool Administration IEP for laboratory engineers iii) Upgrading of VLSI design laboratories iv) Networked PhD Program v) Introduce teaching of various courses on VLSI Design & System level design (BE/B.Tech/ME/M.Tech/ PhD) vi) Prototyping and Siliconization under India Chip Programme/ Chip Center vii) Knowledge exchange programme viii) Web based Dissemination of educational material and setting up of C2S Website and Mirror sites ix) Support for attending national/international conferences xi) Attend Conference/ Workshops / symposium/ ZOPP workshop	i) Design of Board Level Designs using FPGAs ii) Attend Instruction Enhancement Program (IEP) for faculty of PIs and tool Administration IEP for laboratory engineers iii) Setting up of VLSI design laboratories iv)Introduce teaching of various courses on VLSI Design & System level design (BE/B.Tech/ME/M.Tech) v) Prototyping and Siliconization under India Chip Programme/ Chip Center vi)Knowledge exchange programme vii) Web based Dissemination of educational material and setting up of C2S Website and Mirror sites viii) Support for attending national/international conferences xii) Attend Conference/ Workshops / symposium/ ZOPP workshop

Annexure-II

List of implementing Agencies- Proposed RC-PI Clusters

List of Resource Centres (RCs) and their association with Participating Institutions (PIs)

S. No.	Cluster of RC & PI			S. No.	Cluster of RC & PI		
(i)	1. **CEERI Pilani-RC & Program Coordination Institute**			(ii)	7. **IIT Delhi**	-	**RC**
	2. IIT Jodhpur	-	PI		8. IIT Mandi	-	PI
	3. NIT Kurukshetra	-	PI		9. NIT Srinagar	-	PI
	4. ABV IIITM Gwalior	-	PI		10. NIT Delhi	-	PI
	5. NIT Hamirpur	-	PI		11. IIT Ropar	-	PI
	6. Thapar University, Patiala	-	PI		12. Indira Gandhi Technical University for Women, Delhi	-	PI
(iii)	13. **IIT Kanpur**	-	**RC**	(iv)	19. **IIT KGP**	-	**RC**
	14. MNNIT Allahabad	-	PI		20. IIT Bhubaneswar	-	PI
	15. IIT Patna	-	PI		21. IIEST Howrah	-	PI
	16. IIT Varanasi	-	PI		22. Jadavpur University	-	PI
	17. IIIT Allahabad	-	PI		23. University of Calcutta	-	PI
	18. NIT Durgapur	-	PI		24. NIT Sikkim	-	PI
(v)	25. **IISc. Bangalore**	-	**RC**	(vi)	31. **IIT Bombay**	-	**RC**
	26. PSG College of Technology, Coimbatore	-	PI		32. SV-NIT Surat	-	PI
	27. NIT Warangal	-	PI		33. MA-NIT Bhopal	-	PI
	28. IIT Hyderabad	-	PI		34. SGSITS Indore	-	PI
	29. NIT Surathkal	-	PI		35. IIT Gandhinagar	-	PI
	30. NIT Rourkela	-	PI		36. IIT Indore	-	PI
(vii)	37. **IIT Madras**	-	**RC**	(viii)	43. **IIT Guwahati**	-	**RC**
	38. NIT Calicut	-	PI		44. NIT Manipur	-	PI
	39. NIT Silchar	-	PI		45. NIT Agartala	-	PI
	40. NIT Puducherry	-	PI		46. NIT Arunachal Pradesh (Yupia)	-	PI
	41. IIIT Kanchipuram	-	PI		47. NIT Meghalaya	-	PI
	42. NIT Tiruchirappalli	-	PI		48. NIT Nagaland	-	PI
					49. NIT Mizoram	-	PI
(ix)	50. **VNIT Nagpur**	-	**RC**	(x)	55. **IIT Roorkee**	-	**RC**
	51. MNIT Jaipur	-	PI		56. NIT Uttarakhand	-	PI
	52. PDPM IIIT (D&M) Jabalpur	-	PI		57. NIT Goa	-	PI
	53. NIT Raipur	-	PI		58. NIT Patna	-	PI
	54. NIT Jamshedpur	-	PI		59. DBRA NIT Jalandhar	-	PI
	60. DeitY Society*	-	PI				

* To be identified and associated with an RC based on geographical proximity

Annexure-III

Expected Deliverables in 'Special Manpower Development Programme for Chips to System Design'

		60 institutions being covered in Special Manpower Development Programme for Chips to System Design			
S.No.	Institution category Outputs Numbers	SMDP II- RCs (5 IITs + IISc + CEERI Pilani)	SMDP II- PIs (NITs/Others)	New IITs	New NITs/IIITs/ Others
		7	25	8	20
1.	SOC/ ASICs/ FPGA Boards for societal applications	SOCs/s/Sub-s		(11x 2=22)	Board design – FPGAs 30
		10	(22x2=44) ASICs 70*		
2.	Manpower: Teaching courses on VLSI Design & System level design	**50680 Students**			
i.	Type I (Ph.D) under Networked PhD Program	300			
ii.	Type II (M. Tech in VLSI)	4460			
iii.	Type III (M. Tech in Computer/ Communication etc. with at least two VLSI courses / minor project in VLSI)	8310			
iv.	Type IV (B. Tech with at least two VLSI Courses / minor project in VLSI)	37610			
3.	Instruction Enhancement Program (IEP)	15 Instruction Enhancement Program in various topics as listed in DPR would be conducted for faculty of RCs/PIs			
4.	Prototyping and Siliconization under India Chip Programme, and establishment of a Chip Centre	4 MPW runs per year for the implementing agencies. 50 best designs (from institutions not covered under the program) identified as per selection basis will be siliconized and prototype given back to the respective institutions. For undertaking siliconozation of chips a dedicated center having capability to integrate MPW would be set up to service all ASIC prototyping and fabrication including testing.			
5.	Knowledge exchange Program	5-10 collaborative research & development project with foreign universities would be undertaken keeping system development in mind, 25-30 IPs would be generated / protected and about 300-1000 papers would be published.			
6.	Setting up / upgrading of VLSI Design Laboratories	VLSI Design lab consisting of hardware / software / EDA Tools would be set up at all the implementing agencies.			
7.	Web based dissemination	All educational materials developed under the program would be disseminated through the website. The web based project administration would be provided to all the institutions participating in the program.			
8.	Workshop/ Symposium/ZOPP	Workshop/ Symposium would be conducted for identification of industry oriented projects as well as projects of societal relevance. ZOPP workshop would be conducted for all the implementing agencies to give an insight to all the Chief Investigators of the program on all the activities carried out by all the institutions participating in the program.			

Annexure- IV

Expected Manpower to be Generated

Year	1st	2nd	3rd	4th	5th	Total
Type IV	143	143	143	143	143	715
Type III	45	45	45	45	45	225
Type II	20	20	20	20	20	100
Type I	02	02	02	02	02	10

Annexure V

No. 9(1)/2014-MDD
Government of India
Ministry of Communications and Information Technology
Department of Electronics and Information Technology
R&D in Electronics Group
(Microelectronics Development Division)

New Delhi – 110003
Dated: 15th December, 2014

ADMINISTRATIVE APPROVAL

Subject : Administrative Approval for the execution of the Project entitled "Special Manpower Development Programme for CHIPS to System Design (SMDP-C2SD)" to be implemented by Ten Resource Centres (RCs) and Fifty Participating Institutions (PIs).

Sir,

I am directed to convey the Administrative Approval of the Competent Authority for the implementation of the above subject project at the total estimated cost of Rs. 99.72 Crores (Rupees Ninety Nine Crore and Seventy Two Lakh only) over a period of five years. The details of the project are given in the Annexure enclosed.

2. This issues with the approval of the Secretary, Department of Electronics and Information Technology vide OPA No. 3049131 dated 10th December, 2014 and the concurrence of JS & FA, DeitY vide OPA No. 3049131 dated 09th December, 2014.

RJuneja
(R. K. JUNEJA)
Deputy Director

1. Pay and Accounts Office, DeitY.
2. The Director, Office of the Director General of Audit, Post & Telecommunication, Shamnath Marg, Civil Lines, New Delhi – 110054.
3. Drawing & Disbursing Section, DeitY.
4. Finance Section, DeitY.
5. Dr. Chandra Shekhar, Director, Central Electronics Engineering Research Institute (CEERI), Pilani-333031.
6. Dr. Debashis Dutta, Senior Director & Group Coordinator (R&D in Electronics), DeitY.
7. Shri Sunil Alag, Scientist 'F' & Head, Microelectronics Development Division, DeitY.
8. Shri A. K. Arora, Scientist 'F' & Head, HRD Division, DeitY.
9. Project File.
10. Master Sanction File.

ANNEXURE TO THE ADMINISTRATIVE APPROVAL No. 9(1)/2014-MDD DATED 15th DECEMBER, 2014.

1. Name of the Project : Special Manpower Development Programme for CHIPS to System Design (SMDP-C2SD)

2. Objectives :

   i. Bring in a culture of System on Chip / System designing by developing working prototypes with societal applications using mostly in-house designed ASICs / ICs.

   ii. Capacity building in the area of VLSI/ Microelectronics and Chip to System Development.

   iii. Broaden the base of ASIC / IC designing in the country.

   iv. Broaden the R&D base of Microelectronics / Chip to System through 'Networked PhD' Program.

   v. Promote 'Knowledge Exchange Program'.

   vi. Protection of "Intellectual Property" generated in the programme.

3. Area of Coverage — The major components of the Programme are:

   i) Design, development and demonstration of Working Prototype of Systems /sub-systems / System on Chip (SoCs)

   ii) Design of Application Specific Integrated Circuits (ASICs) and Board Level Designs using FPGAs

   iii) Instruction Enhancement Program (IEP) for faculty of PIs and tool Administration IEP for laboratory engineers of RCs and PIs

   iv) Setting up/upgrading of VLSI design laboratories at all institutions

   v) Introduce teaching of various courses on VLSI Design & System level design

RJuneja

-26-

8.Total Product Outlay – Rs. 99.72 Crore

Break-up of expenditure on various activities / head (All figures in Rs. Crores)

S.No.	Description	Expenditure for 5 years	Ist. Year	2nd. Year	3rd. Year	4th. Year	5th. Year
1.	**Capital equipments**: H/W, UPS, EDA Tools for VLSI labs, Other Equipments (including prototyping testing charges, centralized procurement charges, duty component, if any) for all 60 institutions	**30.00**	14.00	12.00	3.00	1.00	0
2.	**Manpower**	**41.00**	6.72	7.40	8.13	8.94	9.81
2.1	*Manpower for RCs & PIs for VLSI Design Activity*						
2.1.1	*Salary for Lab Engineers (60 institutions)*	***15.00***	*2.46*	*2.71*	*2.98*	*3.27*	*3.58*
2.1.2	*Salary for one guest/temporary lecturer (for 40 institutions excluding IITs, IISc, CEERI & DietY Society)*	***12.00***	*1.97*	*2.17*	*2.38*	*2.62*	*2.86*
2.1.3	*Salary for Research/ Project Associate/Assistance (for 60 institutions)*	***9.00***	*1.47*	*1.62*	*1.78*	*1.96*	*2.17*
2.2	*Manpower for - Chip Integration Activities and Development of SoCs / System / Sub-System under Sub-Activity Chip to System development*	***5.00***	*0.82*	*0.90*	*0.99*	*1.09*	*1.20*
2.3	*Stipend for 300 PhDs Students - to be taken separately from HRD programme of DeitY**	*	*	*	*	*	*
3.	**India Chip Program : Chip fabrication, MPW runs etc.**	**2.50**	0.50	0.50	0.50	0.50	0.50
4.	**Program Coordination Institute (Travel, Salary for contract staff, equipment, consumable etc.)**	**3.50**	1.32	0.54	0.57	0.55	0.52
5.	**Instruction Enhancement Program**	**1.00**	0.20	0.20	0.20	0.20	0.20
6.	**Miscellaneous**	**1.12**	0.23	0.23	0.22	0.22	0.22
7.	**Website Activity**	**0.50**	0.30	0.05	0.05	0.05	0.05
8.	**Consumables**	**3.60**	0.72	0.72	0.72	0.72	0.72
9.	**Contingencies**	**3.00**	0.60	0.60	0.60	0.60	0.60
10.	**Travel & training (including International travel/ bilateral cooperation)**	**4.50**	0.50	1.00	1.00	1.00	1.00
11.	**Overheads**	**9.00**	1.57	1.64	1.77	1.92	2.10
	Total Project Cost	**99.72**	**26.66**	**24.88**	**16.76**	**15.7**	**15.72**

*Funds for Networked PhDs to be provided separately from PhD Schemes of DeitY "Scheme to give a thrust to research in areas of Electronics System Design and Manufacturing and IT/IT Enabled Services (ITES)"

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vi) Networked PhD Program

vii) Prototyping and Siliconization under India Chip Programme/ Chip Center

viii) Knowledge exchange programme

ix) Web based Dissemination of educational material and setting up of C2S Website and Mirror sites

x) Support for attending national/international conferences

xi) Organizing Conference/ Workshops / symposium/ ZOPP workshop

4. Location : The programme would be implemented at 10 Resource Centres (RCs) and 50 Participating Institutes (PIs). The association of RCs with PIs is indicated at Appendix A

5. Implementation Modalities : The Implementing Agencies (RCs & PIs) would submit proposals for consideration of National Steering Committee (NSC)*. Based on the recommendations of the NSC, the Program Coordination Institute (PCI), CEERI, Pilani would make the funds available to the Resource Centres (RCs) and Participating Institutions (PIs) accordingly.

6. Name of the Implementing Agencies : 10 Resource Centres (RCs) and 50 Participating Institutes (PIs) (The association of RCs with PIs is indicated at Appendix A).

7. Total Project duration : Five Years.

(i) Expected date of commencement : 15th December, 2014

(ii) Expected date of completion : 14th December, 2019

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9. Mode and extent of funding :

i) Budgetary support

a) Grants-in- aid : Rs. 99.72 Crore from DeitY

b) Loan (If Loan, terms & conditions for grant of loan to be stipulated) : NIL

ii) Internal generation : NIL

iii) Other funding agencies : NIL

10. Stages for the release of payment :

(Rs. in Crores)

Release No.	Pre-condition/ Stage of Implementation	Documentation to be supplied by the Implementing Agency	Implementing Agency /(Programme Coordination Institute)	Amount to be released
1st installment	Initiation of the Project	i) Memorandum of Understanding ii) Acceptance of the Terms and Conditions Governing Grants-in-aid	CEERI, Pilani	Rs. 26.66
2nd installment	Release would be based on the progress, milestones achieved and recommendations of the NSC/PRSG**.	i) Utilization Certificate for the previous Grants ii) Technical and Financial Progress Report iii) Statement of Accounts	CEERI, Pilani	Rs. 24.88
3rd installment	Release would be based on the progress, milestones achieved and recommendations of the NSC/PRSG**.	i) Utilization Certificate for the previous Grants ii) Technical and Financial Progress Report iii) Statement of Accounts	CEERI, Pilani	Rs. 16.76

Rjuneja

4th installment	Release would be based on the progress, milestones achieved and recommendations of the NSC/PRSG**.	i) Utilization Certificate for the previous Grants ii) Technical and Financial Progress Report iii) Statement of Accounts	CEERI, Pilani	Rs. 15.70
5th installment	Release would be based on the progress, milestones achieved and recommendations of the NSC/PRSG**.	i) Utilization Certificate for the previous Grants ii) Technical and Financial Progress Report iii) Statement of Accounts	CEERI, Pilani	Rs. 15.72

* The Office Memorandum for the Composition and Terms of Reference of National Steering Committee is being issued separately.
**The Programme Coordination Institute (PCI), CEERI, Pilani would make the funds available to the Resource Centres (RCs) and Participating Institutions (PIs).

The foreign travel under the project would be subject to recommendations of the PRSG and approval of National Steering Committee (NSC) taking into account the austerity instructions on foreign travel issued by the Ministry of Finance.

RJuneja
(R. K. JUNEJA)
Deputy Director

List of implementing Agencies

List of Resource Centres (RCs) and their association with Participating Institutions (PIs)

S. No.	Cluster of RC & PI			S. No.	Cluster of RC & PI		
(i)	1. CEERI Pilani-RC & Program Coordination Institute			(ii)	7. IIT Delhi	-	RC
	2. IIT Jodhpur	-	PI		8. IIT Mandi	-	PI
	3. NIT Kurukshetra	-	PI		9. NIT Srinagar	-	PI
	4. ABV IIITM Gwalior	-	PI		10. NIT Delhi	-	PI
	5. NIT Hamirpur	-	PI		11. IIT Ropar	-	PI
	6. Thapar University, Patiala	-	PI		12. Indira Gandhi Technical University for Women, Delhi	-	PI
(iii)	13. IIT Kanpur	-	RC	(iv)	19. IIT KGP	-	RC
	14. MNNIT Allahabad	-	PI		20. IIT Bhubaneswar	-	PI
	15. IIT Patna	-	PI		21. IIEST Howrah	-	PI
	16. IIT Varanasi	-	PI		22. Jadavpur University	-	PI
	17. IIIT Allahabad	-	PI		23. University of Calcutta	-	PI
	18. NIT Durgapur	-	PI		24. NIT Sikkim	-	PI
(v)	25. IISc. Bangalore	-	RC	(vi)	31. IIT Bombay	-	RC
	26. PSG College of Science & Technology, Coimbatore	-	PI		32. SV-NIT Surat	-	PI
	27. NIT Warangal	-	PI		33. MA-NIT Bhopal	-	PI
	28. IIT Hyderabad	-	PI		34. SGSITS Indore	-	PI
	29. NIT Surathkal	-	PI		35. IIT Gandhinagar	-	PI
	30. NIT Rourkela	-	PI		36. IIT Indore	-	PI
(vii)	37. IIT Madras	-	RC	(viii)	43. IIT Guwahati	-	RC
	38. NIT Calicut	-	PI		44. NIT Manipur	-	PI
	39. NIT Silchar	-	PI		45. NIT Agartala	-	PI
	40. NIT Puducherry	-	PI		46. NIT Yupia	-	PI
	41. IIIT Kanchipuram	-	PI		47. NIT Meghalaya	-	PI
	42. NIT Tiruchirappalli	-	PI		48. NIT Nagaland	-	PI
					49. NIT Mizoram	-	PI
(ix)	50. VNIT Nagpur	-	RC	(x)	55. IIT Roorkee	-	RC
	51. MNIT Jaipur	-	PI		56. NIT Uttarakhand	-	PI
	52. PDPM IIIT (D&M) Jabalpur	-	PI		57. NIT Goa	-	PI
	53. NIT Raipur	-	PI		58. NIT Patna	-	PI
	54. NIT Jamshedpur	-	PI		59. DBRA NIT Jalandhar	-	PI
	60. DeitY Society*	-	PI				

* To be identified and associated with an RC based on geographical proximity

ANNEXURE-VI

Department of Electronics & Information Technology(DeitY)
Ministry of Communications & IT
Government of India

Terms & Conditions governing Grant-in-aid for funding R&D Projects

I. Applicability

These terms & conditions apply to the institutions who receive grant-in-aid from DeitY for undertaking R&D projects.

II. Definition

In these instructions:

i. The "institution" means any technical, scientific or academic establishment where research work is carried out through funding by DeitY. (including R&D Laboratories, Autonomous Scientific Societies etc.)
ii. "Inventor" means researcher/ employee of the Institution whose duties involve carrying out scientific or technical research work in an R&D project funded by DeitY.
iii. "Intellectual Property Rights" include patents, Trademarks, registered designs, copyrights and layout design of integrated circuits.

III. General Conditions

1. The grant is for undertaking the specific project as approved by DeitY and shall be subject to the following conditions:

   i. The grant shall be spent for the project within the specified time
   ii. Any portion of the grant which is not ultimately required for expenditure for the approved purposes shall be duly surrendered to DeitY.

2. For a project being executed by DeitY grant, Application by grantee institution for any other financial assistance or receipt of grant/loan from any other Agency/Ministry/Department for the same project should have the prior permission/approval of DeitY.

3. The grantee institution is not allowed to entrust the implementation of this project for which grant-in-aid is received, to another institution and to divert the grant-in-aid received from DeitY as assistance to the later institution. However available IP core etc. could be procured with due payment of license fee as per the recommendations of PRSG.

4. The investigator(s) should not enter into collaboration with a foreign party (individual/academic institution/ industry) in execution of this project without prior approval of DeitY.

5. The grantee institution(s) shall make all efforts to protect the Intellectual Property Rights (IPR) being generated through the research project and follow the section "Guidelines for IPR" as laid by DeitY.

6. The grantee institution, while undertaking the technology transfer/commercialization activities, shall follow the procedure laid down by their own institution. In case there is no such procedure/framework within the grantee institution, a transparent mechanism based on the guidelines indicated at section "Guidelines for Technology Transfer/ commercialization" shall be followed.

7. In case the grantee institution does not license the patent/ commercialise the technology within a period of 5 years from the time of obtaining the patent/ development of technology, the grantee institution will make available the patent/technology in public domain for usage by Indian companies/MSMEs/startups/entrepreneurs/citizens.

8. The Grantee institution should indemnify DeitY from any legal and/or financial incumbrance arising out of any infringement of IPR/ licensing of IPR/ technology transfer/ commercialization.

9. Any dispute on any matter related to the implementation of the project, the decision of Secretary, DeitY, shall be final and binding on the grantee institution.

10. DeitY reserves the right to modify these terms and conditions governing the grant-in-aid from time to time reflecting the directions of the Government of India.

IV. Monitoring & Review of the project

DeitY shall appoint a Project Review and Steering Group (PRSG) comprising of representatives from DeitY and other experts to periodically review and monitor the technical and financial status of the project. PRSG will periodically monitor the project in all respects including technical and financial progress of the project.

V. Acquisition & Management of Assets

1. The grantee institution shall maintain an audited record in the form of a register in the prescribed proforma for permanent, semi-permanent assets acquired solely or mainly out of the DeitY grant. The applicable procedures for procurement shall be followed for acquisition of assets.

2. The assets referred to above will be the property of DeitY and should not, without prior sanction of DeitY, be disposed off or encumbered or utilised for the purposes other than those for which the grant has been sanctioned;

3. The grantee institution shall send a list of assets referred above to DeitY at the end of each financial year as well as at the time of seeking further instalments of the grant;

4. Should at any time grantee institution cease to exist, such assets etc., shall revert to DeitY;

5. At the conclusion/ termination of the project, the Government of India will be free to sell or otherwise dispose off the assets which are the property of the Government. The Institution shall render to the Government necessary facilities for arranging the sale of these assets. The Government of India has the discretion to transfer the assets to the concerned institution or any other institution if it is considered appropriate.

VI. Utilization of grants and Audit

1. The grantee institution should maintain separate audited account for the project. If it is found expedient to keep a part or whole of the grant in a bank account earning interest, the interest, thus earned should be reported to DeitY. The interest so earned will be treated as a credit to the grantee institution to be adjusted towards future instalment of the grant; DeitY or its nominee/s will have the right of access to the books and accounts of the grantee institution for which a reasonable prior notice would be given;

2. The grantee institution shall render an audited statement of accounts and utilization certificate to DeitY, every year. The audited statement of accounts relating to grants given during financial year together with the comments of the auditor regarding the observance of the conditions governing the grant should be forwarded to the DeitY within six months following the end of the relevant financial year;

3. The utilisation of grant for the intended purposes will be looked into by the Auditor of grantee institution according to the directives issued by the Government of India at the instance of the Comptroller and Auditor General and the specific mention about it will be made in the audit report;

4. The grantee institution shall render progress-cum-achievement reports at interval of not exceeding six months on the progress made on all aspects of the project including expenditure incurred on various approved items during the period.

5. **The grantee institution will refund unspent balance in addition to the interest, if any accrued on the unspent balance in the total outlay of the project.**

6. **Ministry or Department will be at liberty to take appropriate action under the Rule 212(1) of GFR 2005 relating to utilization of funds in the specified time and where such certificate is not received from the grantee within the prescribed time (reference General Financial Rules 2005).**

VII. Guidelines for managing IPRs:

1. The IPR arising out of sponsored project(s) will be with grantee institution(s). While the patent may be taken in the name(s) of inventor(s), the institution(s) shall ensure that the IPR is assigned to institution(s). In cases where the funding/resourcing of researchers have been done jointly with other organizations, the IP rights would be appropriately shared among them.

2. The Government of India/Govt. bodies (including its PSUs, Govt. autonomous societies & section 25 companies) shall have right to obtain a royalty- free license for the Intellectual Property for deployment/use of the same for non-commercial purposes. However, in case, IP is proposed for commercial usage, the terms of licensing may be mutually agreed with the grantee institution(s) possessing IPR.

3. The grantee institution shall submit the financial requirements for filing of IPR as part of the R&D proposal. The contingency head could be used for provisioning of the expenditure for filing of IPR with a ceiling of Rs. 15 Lakhs for the cost of initial filing, but excluding for the annuity fee. International Patent filing will be permitted. The amount will be released based on the recommendations of PRSG constituted by DeitY

for the concerned project. If, for any reason, it is not possible to meet the expenses from the project grant, like in the case of the need for filing of IPR arising after the closure of the project, an application may be made separately by the institution to DeitY for sanction/ reimbursement of the expenses incurred in filing of the IPR.

4. The grantee institution shall inform DeitY about the patents filed/obtained and IPR arising out of the R&D project on annual basis over the project duration and subsequent 5 years period after the project closure.

5. The grantee institution shall provide information to DeitY about trading/ selling/ transferring /licensing the IP rights, within a period of 6 weeks from conclusion of the agreement relating to such a commercial event.

6. The grantee institution shall take appropriate licence in case of export of 'Special Chemicals, Organisms, Materials, Equipment and Technologies' (SCOMET) items as per the prevailing provisions of Foreign Trade Policy from Directorate General of Foreign Trade, under Department of Commerce, Govt. of India.

7. As the R& D is supported by public fund, the grantee institution should ensure that the interests of India and its citizens are fully protected, while licensing of patents/transfer or commercialization of technology.

8. The institution is permitted to retain the benefits and earnings arising out of the IPR for plough back to pursue research/research related activities.

9. Not withstanding the above, DeitY reserves the right to take over ownership of the rights of the Intellectual property arising out of this project, in the interest of the Indian sovereignty, without any compensation to the grantee institution.

VIII. Guidelines for Technology Transfer/commercialization:

The Grantee institution may use the following guidelines in case there is no laid down procedure within their own institution:

1. The transfer of technology may normally be undertaken by the central office of the grantee institution equipped to handle legal issues with regard to technology/ IP licensing.

2. The grantee institution shall constitute a Transfer of Technology (ToT) Committee for evaluation of the applications for ToT and for working the appropriate revenues expected out of the ToT

3. Prior to seeking the expression of interest for technology transfer/commercialization, there should be sufficient disclosure of the technical details, features and capabilities of the project through advertisement, publication on the websites of the Institution and of DeitY, and exhibitions, if any held on the related themes during the relevant period. The ToT proposal may be given wide publicity in one national daily besides in journals relating to the theme and by writing to the industry associations related to the theme.

4. Normally, a period of 6 weeks shall be given for interested parties to file their applications relating to Expression of Interest and a format for the application is

attached in Annexure-I which may require customization based on the technology/product/service/prototype proposed to be transferred by the grantee institution.

5. The ToT Evaluation Committee shall undertake a techno-commercial evaluation of the proposals received, adopting a 2-stage process.

6. The ToT committee formed by the grantee institution will work out the cost of ToT on case-to-case basis considering the ground realities like i) development cost of the project ii) market demand of the technology/product iii) ability of the industry to pay for the technology iv) work involved from prototyping to packaging. The cost of capital equipment will be excluded from the total cost of development. Such an estimated cost shall be used as the Internal Bench Mark (IBM) for evaluating the ToT fee and royalty, in Stage 2.

7. After due diligence by the ToT committee a technology transfer/ licensing agreement shall be signed which shall include license of IPRs through existing legal procedures.

8. It is desirable that technology be transferred on a non-exclusive basis. Exclusive licensing should be in the rarest of rare cases based on sufficient justification by the ToT Evaluation Committee and approval by the Head of the institution/ Competent Authority and with the approval of DeitY.

IX. Guidelines for publication of results

1. Investigators wishing to publish technical/ scientific papers based on the research work done under the project, should acknowledge the assistance received from this Department and a copy of the communicated/published paper be sent to DeitY.

2. If the results of research are to be legally protected for the intellectual property, then its publication can be undertaken only after due care is taken for legal protection of the intellectual property rights.

Note :

1. **While submitting the project proposal, a certificate of acceptance of terms and conditions and undertaking to follow the guidelines as above needs to be given by the chief investigator and endorsed by the competent authority of the institution. For any deviation from the terms & conditions and guidelines, the grantee institution will take the permission/approval of the competent authority of DeitY.**

2. **The guidelines for managing IPR and Technology Transfer/ commercialization will not be applicable for the following exceptions and specific approvals have to be taken in respect of IPR and ToT:**

i) **The R&D projects of strategic applications**
ii) **The projects jointly funded by/for strategic departments like defense, space and atomic research etc.**

Invitation for Expression of Interest by grantee institution

(Ref. VIII –Guidelines for Technology Transfer/commercialization para-3 of Terms & conditions governing grant-in-aid for funding R&D Projects)

Instructions to the Bidders to be provided by the grantee institution

The applications are invited for the purpose of Technology Transfer/ commercialization from the organizations with relevant experience.

1. The information to be furnished for Expression of Interest is given in Annexure-I (which may require customization based on the technology/product/service/prototype) being transferred. Interested parties can submit the EOI along with Annexure-I duly filled in with all relevant supporting documents as mentioned in Para 3.0 of EOI document.
2. A Pre-bid meeting of all the Bidders will be convened on ..... The purpose of this meeting will be to clarify the requirements as envisaged by the grantee institution and also to address the queries if any.
3. The EOI's submitted should be sealed properly and marked "EOI for TOT of product/ technology/prototype" so as to reach the following address on or before_____ till _____(Time)

   Details of the contact person

   _____

   _____

   The EOI bids shall be opened on __(date)_____ at _____(time)

   Institution may at its discretion – extend this deadline for the submission of EOI by amending the EOI documents, in which case all rights and obligations of Institution and bidders previously subject to the deadline will thereafter be subjected to the deadline as extended.
4. To assist in the examination, evaluation and comparison of EOI, Institution at its discretion can ask the bidder for the clarification of its EOI. The request for clarification and the response shall be in writing. However no post submission of EOI, clarification at the initiative of the bidder shall be entertained. Authority reserves the right to visit the facilities of the bidders if required.
5. Bidders if they chose, may prior to submitting their Expression of Interest, visit Institution with prior appointment.
6. Bidders may be called for making a presentation before the committee.
7. The grantee institution may visit bidder's facilities for the assessment
8. The grantee institution will issue tender documents to short-listed bidders for the submission of financial bids.
9. At any time before the submission of EOI, the grantee institution may carry out amendment(s) to this EOI document and/ or the schedule. The amendment will be made available on the website (Website details) and will be binding on them. The Authority may at its discretion extend the deadline for the submission of proposals.
10. The Authority reserves the right to accept or reject any application without assigning any reason thereof.

11. Bids that are incomplete in any respect or those that are not consistent with the requirements as specified in this document or those that do not adhere to formats, wherever specified may be considered non-responsive and may be liable for rejection and no further correspondences will be entertained with such bidders.
12. Canvassing in any form would disqualify the applicant.
13. For any clarifications on the Expression of interest document. the following may be contacted through e-mail/FAX/Letter:
    Details of the contact persons

_____

_____

Competent authority
Grantee Institution

Prof. Rajnish Shrivastava
Director
NIT Hamirpur (H.P.)-177005